Z8 Encore!® F6482 Series

Z8F6482 MCU

Programming Specification

PRS001902-1015

PRELIMINARY

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Revision History

Each instance in the following revision history table reflects a change to this document from its previous version. For more details, refer to the corresponding pages or appropriate links provided in the table.

Date	Revision Level	Description	Page Number
Oct 2015	02	Corrected header information.	All
Apr 2015	01	Original issue.	

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Flash Memory Programming Overview

Zilog's Z8F6482 microcontroller, a member of the Z8 Encore! XP family, features Flash program memory selections of 16KB, 32KB, 60KB, and 64KB. By using Flash memory, users have the ability to easily update the code. This Z8 Encore! MCU features an on-chip Flash controller that typically manages the timing of Flash control signals for programming, page erase, and mass erase operations. The Flash controller can also be bypassed to allow direct control of Flash signals via the general purpose input/output (GPIO) pins. Flash memory can be programmed faster by controlling the Flash memory signals directly. Bypassing the Flash controller is beneficial when programming a large number of devices, and is most likely to be used by third party vendors who are developing multi-site gang programmers.

Bypassing the Flash Controller

Flash Controller Bypass Mode is enabled by writing the following three bytes of instruction to the on-chip debugger (OCD) via the DBG interface:

- **80H** –This instruction initiates auto-baud calculation of the DBG interface data and clock rate.
- **F0H** – OCD writes TESTMODE Register command.
- **03H** – Data to be written to the TESTMODE Register. This data enables the Flash Controller Bypass Mode.

Flash Memory Control Signals

Depending on the size (number of bytes) available in Flash memory, interfacing directly to Flash memory uses up to 56 signals:

- 15 signals for the address lines
- 16 signals for data input
- 16 signals for data output
- 10 signals for control operations

The Flash memory control signals are listed and described in Table 6.

Table 6. Flash Memory Control Signals

Signal	Direction	Description
XADR[8:0]	I	X address input selects a row. XADR[8:0] corresponds to the upper 9 bits of the program memory address space (PROGMEM[15:7]). For Z8 Encore! devices with less than 64KB of program memory, the unused upper address bits must be set to 0.
YADR[5:0]	I	Y address input selects one word (two bytes) within a row. {YADR[5:0], 0} corresponds to the lower 7 bits of the program memory address space (PROGMEM[6:0]).
DIN[7:0]	I	Data input
DOUT[7:0]	O	Data output
XE	I	X address enable
YE	I	Y address enable
SE	I	Sense amplifier enable
ERASE	I	Erase enable. This signal is used to select erase operations.
MAS1	I	Mass erase select. This signal is used to distinguish between page erase and mass erase operations.
PROG	I	Program enable. This signal is used to select a program operation.
NVSTR	I	Non-volatile store enable. This signal is used during page erase, mass erase, and programming operations.
TMR	I	This signal should be set to 1 during all operations.
IFREN	I	Information area select
LVE	I	Low voltage read enable. Since the Z8F6482 MCU will control Vcore to be ≥ 1.62V, LVE remains Low for all accesses.

Flash Memory Operations

When bypassing the Flash controller, all Flash memory operations (read, program, page erase, and mass erase) are available. The mode of operation is set by the Flash memory control signals, as described in Table 7.

The selection of the Flash main memory or the Flash information area depends on the IFREN signal, as described in Table 8.

Table 7. Flash Mode Truth Table

Mode	XE	YE	SE	PROG	ERASE	MAS1	NVSTR	TMR	IFREN	LVE
Read (1.62-1.98V)	H	H	H	L	L	L	L	H	L/H[1]	L
Low VDD Read (1.2-1.62V)	H	H	H	L	L	L	L	H	L/H[1]	H
Program	H	H	L	H	L	L	H	H	L/H[1]	L
Page Erase	H	L	L	L	H	L	H	H	L/H[1]	L
Mass Erase	H	L	L	L	H	H	H	H	L/H[1]	L

[1]See Table 8 for IFREN signal operation information.

Table 8. IFREN Signal Truth Table

Mode	IFREN = 1	IFREN = 0
Read	Read Information Area	Read Main Memory
Program	Program Information Area	Program Main Memory
Page Erase	Page Erase Information Area	Page Erase Main Memory
Mass Erase	Mass Erase Information Area and Main Memory	Mass Erase Main Memory

Flash Bypass Mode Register Structure

To use Flash Controller Bypass Mode for all package sizes, the Flash control and data signals must be registered internally. This allows all data access to occur through Port A [7:0]. Three other pins, Port B[2:0], select one of the input data registers or the data output register as shown in Table 9. Control and Data are clocked in to the selected register on the rising edge of Port C5.

Table 9. Registers in Flash Bypass Mode

	Register Select,"SEL" (Port B[2:0])							
Data Input/ Output, "DIO"	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
	Input	**Input**	**Input**	**Input**	**Output**	**Output**	**Input**	**Input**
Port A7	XADR[8]	XADR[0]	DIN[15]	DIN[7]	DOUT[15]	DOUT[7]	XE	TMR
Port A6	XADR[7]	YADR[5]	DIN[14]	DIN[6]	DOUT[14]	DOUT[6]	YE	LVE
Port A5	XADR[6]	YADR[4]	DIN[13]	DIN[5]	DOUT[13]	DOUT[5]	SE	
Port A4	XADR[5]	YADR[3]	DIN[12]	DIN[4]	DOUT[12]	DOUT[4]	IFREN	
Port A3	XADR[4]	YADR[2]	DIN[11]	DIN[3]	DOUT[11]	DOUT[3]	ERASE	
Port A2	XADR[3]	YADR[1]	DIN[10]	DIN[2]	DOUT[10]	DOUT[2]	PROG	
Port A1	XADR[2]	YADR[0]	DIN[9]	DIN[1]	DOUT[9]	DOUT[1]	MAS1	
Port A0	XADR[1]		DIN[8]	DIN[0]	DOUT[8]	DOUT[0]	NVSTR	

Figure 1 illustrates the multiplexed register structure that allows access to all Flash memory signals through GPIO ports.

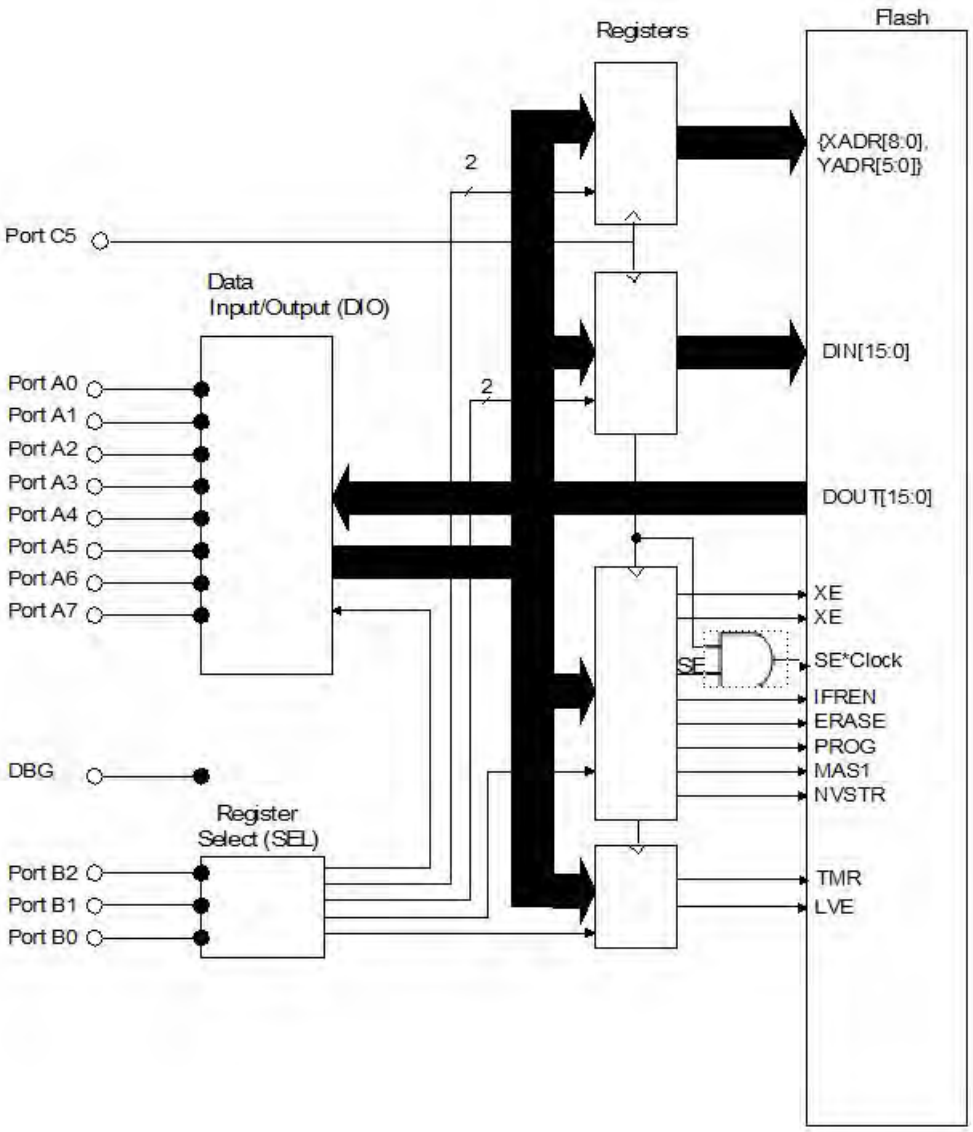


Figure 1. Flash Bypass Mode Register Structure

Bypass Mode Register Read Timing

Register selection is accomplished using the register select pins, Port B[2:0], as detailed in Table 9.

Figure 2 illustrates the timing of a read operation using the Flash controller bypass mode registers. While reading data, output data is latched into the output register on the first clock rising edge after DOUT register selection. The read data is captured externally during the current clock period.

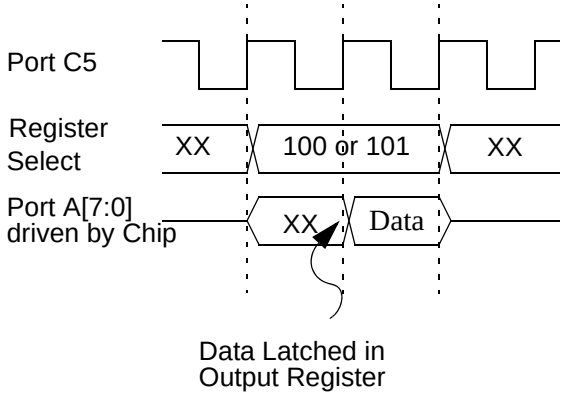


Figure 2. Bypass Mode Register Read Timing

Bypass Mode Register Write Timing

Figure 3 illustrates the timing of a write operation using the Flash Controller Bypass Mode registers. When writing data into the registers, the data is latched on the clock rising edge.

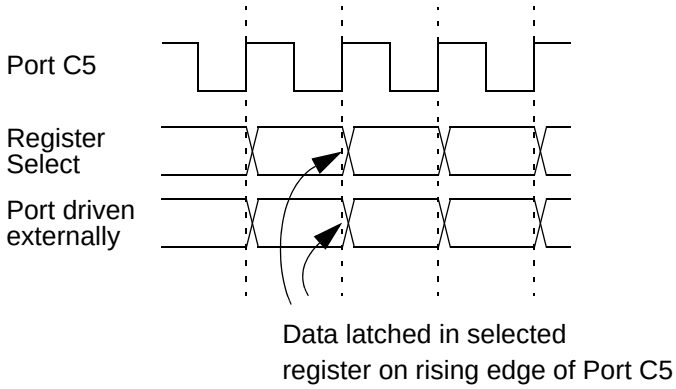


Figure 3. Bypass Mode Register Write Timing

Flash Row Programming

Flash memory can be programmed either as a single word at a time or as a row of words at a time. Multi-word row programming allows programming of up to a full row of Flash memory without incurring all of the programming setup and recovery time for each word. During row programming, the Flash memory's PROG and NVSTR signals are continuously asserted until all words in a row are programmed. This allows the row to be programmed faster than if these signals are deasserted after programming each word.

During row programming, ensure that the cumulative programming high voltage period does not exceed the specification limits for a row.

Flash Memory Timing

Table 10 and Figures 4 through 7 provide detailed timing information on accessing the Flash memory in Flash Controller Bypass Mode.

Table 10. Flash Memory Timing Parameters

Parameter	Symbol	Min.	Max.	Unit
Cycle time	Tcyc	40	-	ns
Address to SE setup time	Tas	2	-	ns
SE access time	Tsa	-	90	ns
Negative pulse width of SE	Tnws	15		ns
Positive pulse width of SE	Tpws	15		ns
PROG/ERASE to NVSTR setup time	Tnvs	5	-	µs
NVSTR hold time	Tnvh	5	-	µs
NVSTR hold time (Mass Erase)	Tnvh1	100	-	µs
NVSTR to program setup time	Tpgs	10	-	µs
Program hold time	Tpgh	20	-	ns
Byte program time	Tprog	20	40	µs
Address / Data setup time	Tads	20	-	ns
Address / Data hold time	Tadh	20	-	ns
Recovery time	Trcv	1	-	µs
Cumulative program high voltage period[1]	Thv	-	8	ms

Table 10. Flash Memory Timing Parameters (Continued)

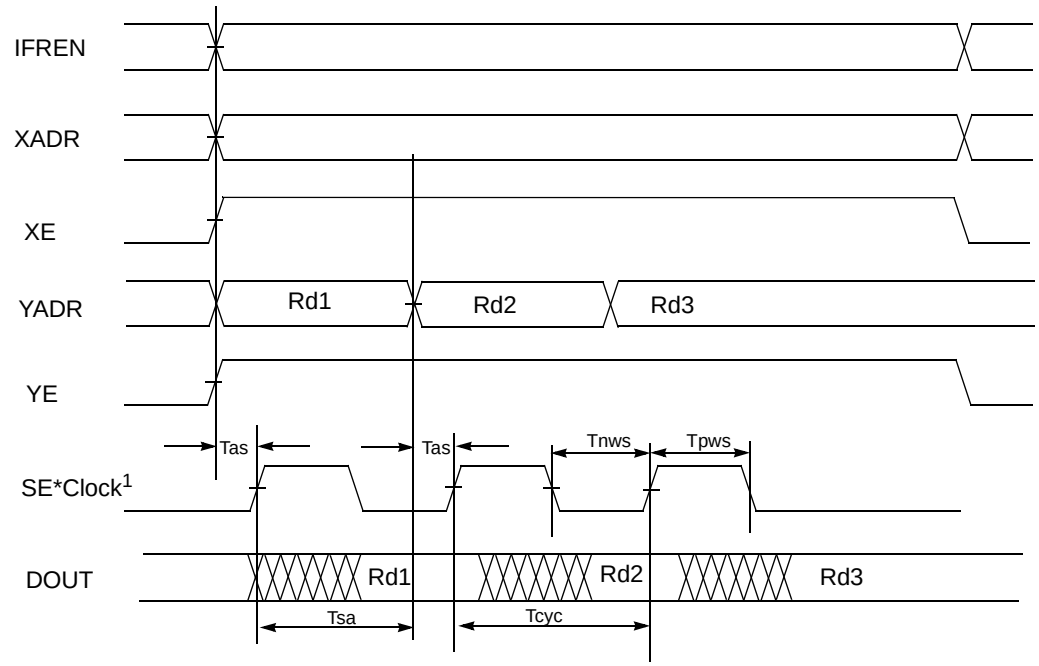
Parameter	Symbol	Min.	Max.	Unit
Erase time	Terase	20	40	ms
Mass Erase time	Tme	20	40	ms

[1]Thv is the cumulative high voltage programming time for a single row before the next erase.

Caution: The same address (byte) cannot be programmed more than twice before the next erase.

Flash Read Timing

Figure 4 illustrates the timing of a read operation from the Flash memory.

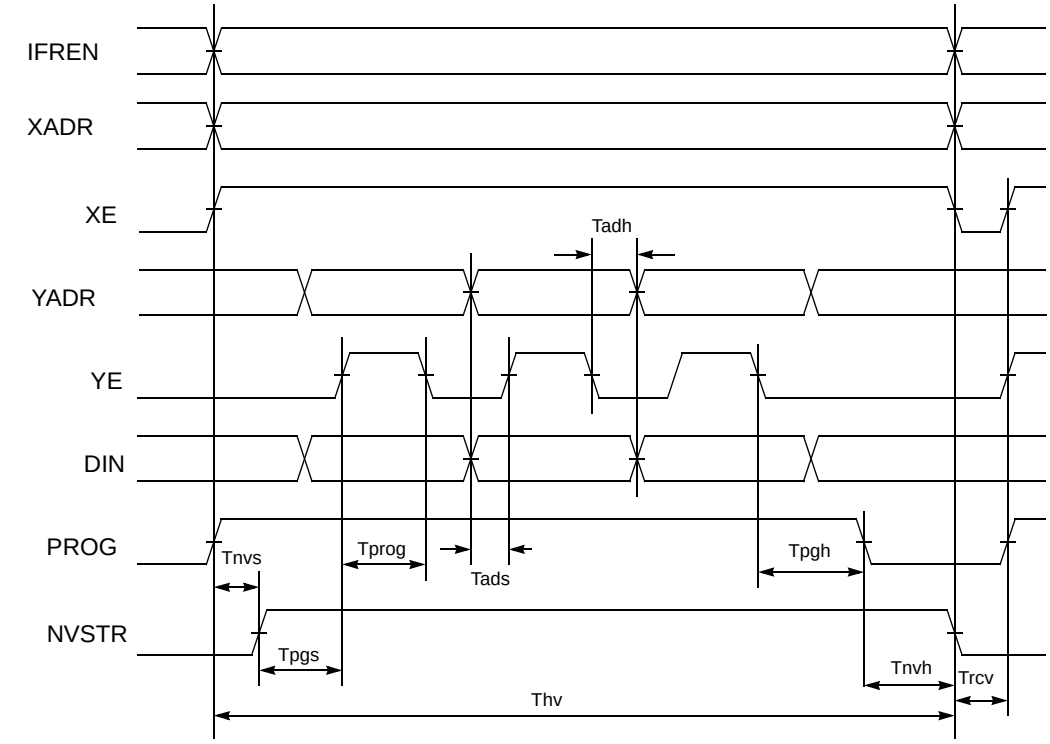


ERASE = 0, MAS1 = 0, NVSTR = 0, TMR = 1, LVE = 0
[1]The SE register bit is anded with the clock during read operations. Due to this, additional SE*clock pulses (not shown) occur when addresses are updated.

Figure 4. Flash Read Timing

Flash Program Timing

Figure 5 illustrates the Flash programming operation for three bytes on a single row. The XADR is unchanged while PROG and NVSTR are high, but the YADR changes three times to identify three different words in a single row.

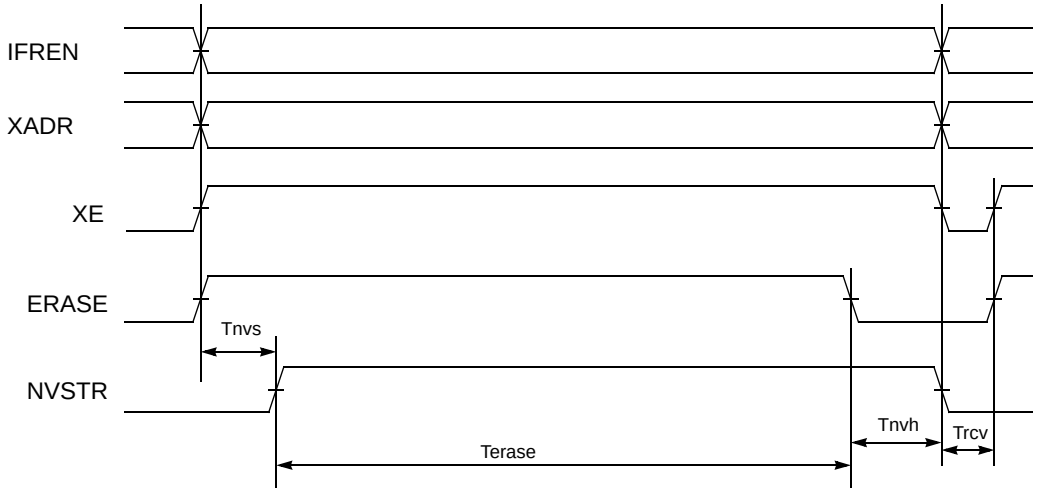


SE = 0, ERASE = 0, MAS1 = 0, TMR = 1, LVE = 0

Figure 5. Flash Word Program Timing

Flash Page Erase Timing

Figure 6 illustrates the timing of a Flash page erase operation.

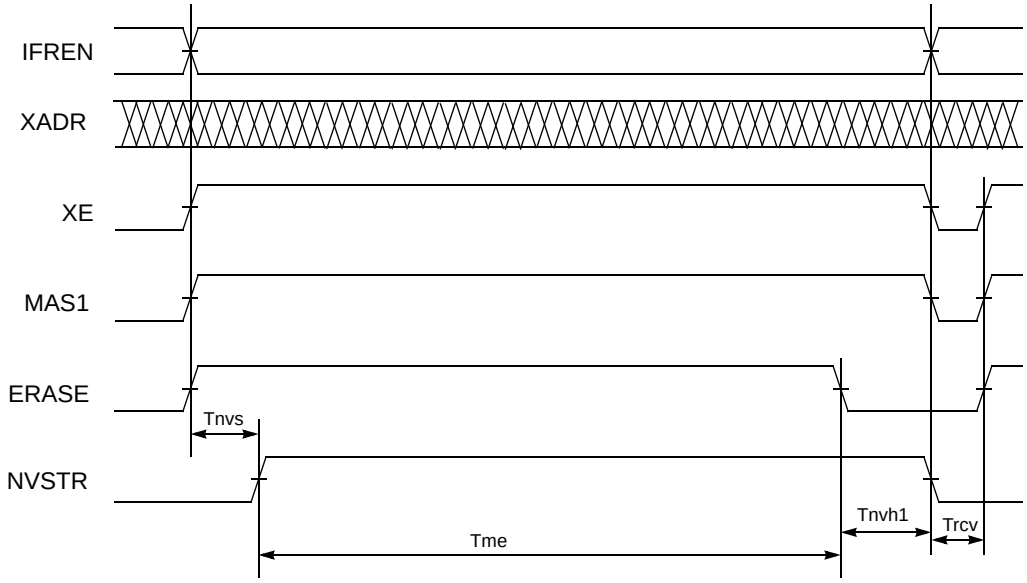


YE = 0, SE = 0, PROG = 0, MAS1 = 0, TMR = 1, LVE = 0, YADR = don't care

Figure 6. Flash Page Erase Timing

Flash Mass Erase Timing

Figure 7 illustrates the timing of a Flash mass erase operation.With IFREN driven high (1), the mass erase operation will erase both the main memory and the information area. With IFREN driven low (0), the mass erase operation will erase only the main memory.



YE = 0, SE = 0, PROG = 0, TMR = 1, LVE = 0, YADR = don't care

Figure 7. Flash Mass Erase Timing

Z8F6482 Flash Programming Flowchart

Figure 8 illustrates an example flowchart for read and write operations.

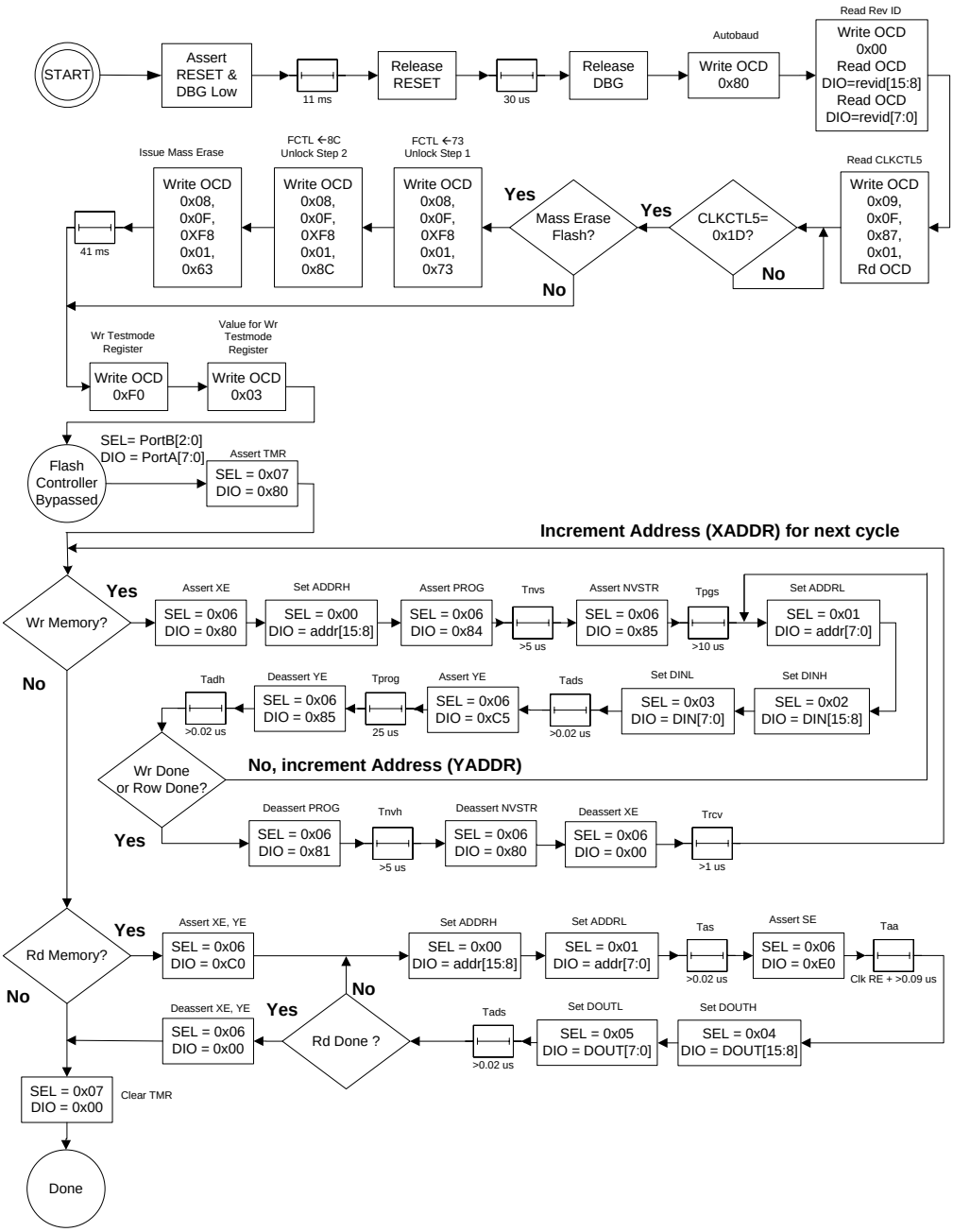


Figure 8. Z8F6482 Flash Gang Programming Flow